CLAIMS

What is claimed is:

1. A thin film Silicon on Insulator (SOI) device comprising a source (101), a gate (103), a drain (102), an SOI layer (104), and a substrate layer (107), the substrate layer being maintained at a potential enough lower than the source so that a parasitic MOS channel (110) is formed between the source and drain; and a Deep N implant layer (201) formed between either the source or drain and the parasitic MOS channel to prevent the flow of current between the source and drain via the parasitic MOS channel when the device is in an off state.

2. The device of claim 1 wherein the Deep N implant layer (201) is formed between the source (101) and the parasitic MOS channel (110).

3. The device of claim 1 wherein the Deep N implant layer (201) is formed between the drain (102) and the parasitic MOS channel (110).

4. A thin film Silicon on Insulator (SOI) device comprising a source (101), a gate (103), a drain (102), an SOI layer (104), and a substrate layer (107), the SOI layer being maintained at a potential enough higher than the source (101) so that a parasitic MOS channel (110) is formed between the source (101) and drain (102); and a Deep P implant layer formed between either the source or drain and the parasitic MOS channel to prevent the flow of current between the source (101) and drain (102) via the parasitic MOS (110) channel when the device is in an off state.

5. The device of claim 1 wherein the Deep P implant layer is formed between the source (101) and the parasitic MOS channel (110).

6. The device of claim 1 wherein the Deep P implant layer is formed between the drain (102) and the parasitic MOS channel (110).

7. A method of isolating the source and drain of an MOS device to avoid a parasitic MOS channel being formed comprising adding a double ionized 31P++ implant to form a deep N layer (201) beneath the drain (102) or source (101) of the MOS device, thereby preventing current flow across a parasitic MOS channel (110) formed in said MOS device when the device is in an off state.

8. The method of claim 7 wherein said device includes a buried oxide layer, and wherein said parasitic MOS channel forms at or near the buried oxide layer (106) – silicon layer (104) interface.

9. The method of claim 7 wherein the doping concentration of the deep N layer (201) is approximately one order of magnitude higher than that of the NWell layer on the device.

10. A CMOS device comprising source (101) and drain (102) regions adjacent to a buried oxide layer (106) and separated by a gate region (103), the buried oxide layer (106) being adjacent to a substrate layer (107), and an implant layer (201) of particles directly below the drain (102) or source (101) such that when the difference in potential between the substrate and the source exceeds 30 volts, a parasitic MOS channel (110) is induced across the gate region and the implant layer (201) isolates said parasitic MOS channel (110) from said drain region (102) to thereby prevent current flow between said source (101) and drain (102) via said parasitic MOS channel (110).

11. The device of claim 10 wherein the ionized particles are implanted using approximately 200keV of energy.